**Background & Model Choice**

**1.1 What makes a memristor useful**

A memristor links charge and flux, giving it a conductance that “remembers” the time-integral of the applied stimulus. This property makes it an ideal analogue synapse for neuromorphic circuits because its conductance can encode a weight that changes gradually with pre-/post-synaptic spikes through mechanisms such as STDP [pmc.ncbi.nlm.nih.gov](https://pmc.ncbi.nlm.nih.gov/articles/PMC3062969/?utm_source=chatgpt.com). HP’s 2008 TiO₂ device was the first nanoscale demonstration [nature.com](https://www.nature.com/articles/nature06932?utm_source=chatgpt.com), and subsequent debate only strengthened interest in scalable models [wired.com](https://www.wired.com/2012/07/memristors?utm_source=chatgpt.com)[wired.com](https://www.wired.com/2008/04/scientists-prov?utm_source=chatgpt.com).

**1.2 Why the Biolek model**

The original linear-drift (Strukov) model exhibits unphysical boundary behaviour at x = 0/1. Biolek et al. introduced a *window function* that suppresses drift as the internal state approaches its limits while keeping the model algebraically simple and SPICE-friendly [radioeng.cz](https://www.radioeng.cz/fulltexts/2009/09_02_210_214.pdf?utm_source=chatgpt.com)[researchgate.net](https://www.researchgate.net/publication/26625012_SPICE_Model_of_Memristor_with_Nonlinear_Dopant_Drift?utm_source=chatgpt.com). The same formulation lends itself to a compact Python ODE solver and yields stable, bounded dynamics.

**Governing equations** (current-controlled variant):

***M(x) = R\_on \* x + R\_off \* (1 - x)***

***dx/dt = k \* I \* F(x) where F(x) = 1 - (2x - 1)^(2p), 0 ≤ x ≤ 1***

**2 Implementation Highlights**

| **Step** | **What happens** | **Key parameters** |
| --- | --- | --- |
| 1. Define constants | Set Ron, Roff, D, mu, and compute k | Ron = 100 Ω, Roff = 16kΩ, D = 10nm, μ = 10⁻¹⁴ m²/Vs |
| 2. Drive waveform | Generate V(t) = V₀·sin(2πft) | V₀ = 1V, f = 1kHz |
| 3. Time stepping | Euler update x[n+1] = x[n] + dx·dt | dt = 0.1 µs, p = 2 |
| 4. Record data | Store V(t), I(t) to plot I–V | Confirm pinched hysteresis loop |

The full code—including the plot you see above—was executed live (see notebook cell). To try different scenarios, simply tweak **Ron/Roff**, **frequency**, or **window-order p** in the first cell.

Replace the window() line with the Biolek‐window subcircuit in the Radioengineering paper’s Appendix A [radioeng.cz](https://www.radioeng.cz/fulltexts/2009/09_02_210_214.pdf?utm_source=chatgpt.com), instantiate it in LTspice, and excite it with the same sinusoid. You’ll obtain an identical hysteresis lobe.

**3 Results & Discussion**

**3.1 Pinched hysteresis verified**

The simulated loop shows the hallmark “figure-eight” pinched at the origin—positive current in quadrant I, negative in III—confirming correct memristive behaviour (zero crossing at I = V = 0) [researchgate.net](https://www.researchgate.net/figure/Typical-i-v-characteristic-of-memristor-1-22-The-pinched-hysteresis-loop-is-due-to_fig1_257351781?utm_source=chatgpt.com). Increasing frequency would shrink the lobe area as the state variable fails to follow the stimulus in time, a well-known frequency-compression effect.

**3.2 Parameter sensitivity**

* **R\_ON / R\_OFF ratio:** A larger contrast fattens the loop but can cause numerical stiffness; use a smaller Δt if you go beyond 1:10⁵.
* **Window order p:** Higher p clamps x near 0/1 more aggressively, making the loop thinner but improving device endurance [cyakopcic1.files.wordpress.com](https://cyakopcic1.files.wordpress.com/2014/02/memristor-spice-modeling.pdf?utm_source=chatgpt.com).
* **Ion mobility μ:** Scales the slope of the minor axis; in physical devices μ varies with fabrication chemistry [knowm.org](https://knowm.org/memristor-models-in-ltspice/?utm_source=chatgpt.com).

**3.3 Toward STDP learning**

To emulate STDP, drive the memristor with paired pre-/post-synaptic pulses (e.g., 100-ns triangular spikes). The integral of voltage over each pair adjusts x according to spike timing, reproducing potentiation/depression curves similar to those reported by Jo *et al.* [pmc.ncbi.nlm.nih.gov](https://pmc.ncbi.nlm.nih.gov/articles/PMC3062969/?utm_source=chatgpt.com). You can implement this by swapping the sinusoid for two rectangular pulses with controllable delay and observing ΔM.

**4 How to Report Your Findings**

1. **Introduction** – Briefly review memristor theory (cite Chua 1971 and HP 2008).
2. **Model** – Present Biolek equations; justify window choice.
3. **Simulation Setup** – List parameters, solver, time base.
4. **Results** – Embed the I-V plot (or SPICE screenshot) and tabulate Ron/Roff evolution.
5. **Discussion** – Analyse loop shape, frequency effects, parameter sweeps.
6. **Neuromorphic Relevance** – Tie results to synaptic plasticity (STDP, Hebbian learning).
7. **Conclusion** – Summarise key insights and potential hardware extensions.

Feel free to copy-paste the structure above or adapt it to your formatting preferences (18-pt headings, **bold** emphasis) per your documentation style guide.

**5 References**

1. Biolek, D. *et al.* “SPICE Model of Memristor with Nonlinear Dopant Drift.” Radioengineering 18 (2), 2009. [radioeng.cz](https://www.radioeng.cz/fulltexts/2009/09_02_210_214.pdf?utm_source=chatgpt.com)
2. ResearchGate figure of typical memristor pinched hysteresis. [researchgate.net](https://www.researchgate.net/figure/Typical-i-v-characteristic-of-memristor-1-22-The-pinched-hysteresis-loop-is-due-to_fig1_257351781?utm_source=chatgpt.com)
3. Jo, S. H. *et al.* “Spike-Timing-Dependent Plasticity of a Synapse Induced by Memristive Devices.” Frontiers in Neuroscience 4, 2010. [pmc.ncbi.nlm.nih.gov](https://pmc.ncbi.nlm.nih.gov/articles/PMC3062969/?utm_source=chatgpt.com)
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5. Knowm.org. “Memristor Models in LTspice.” 2017. [knowm.org](https://knowm.org/memristor-models-in-ltspice/?utm_source=chatgpt.com)
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7. Wouters, D. “Fundamentals of Memristors.” ESA ACT Workshop slides, 2014. [esa.int](https://www.esa.int/gsp/ACT/doc/EVENTS/memristor_workshop/ACT-NAN-0415_2_wouters_memristors_DW_final.pdf?utm_source=chatgpt.com)
8. LyeGuanYan/Memristor GitHub project: multiple SPICE and Verilog-A models. [github.com](https://github.com/LyeGuanYan/Memristor?utm_source=chatgpt.com)
9. Cyakopcic, C. “Memristor SPICE Modeling.” LTspice tutorial PDF, 2013. [cyakopcic1.files.wordpress.com](https://cyakopcic1.files.wordpress.com/2014/02/memristor-spice-modeling.pdf?utm_source=chatgpt.com)
10. Wired Magazine. “Wonks Question HP's Claim to Computer-Memory Missing Link.” 2012. [wired.com](https://www.wired.com/2012/07/memristors?utm_source=chatgpt.com)
11. Wired Magazine. “Scientists Create First Memristor: Missing Fourth Electronic Circuit Element.” 2008. [wired.com](https://www.wired.com/2008/04/scientists-prov?utm_source=chatgpt.com)

**Next steps:**

* Sweep frequency to show lobe shrinkage.
* Replace the sinusoid with paired spikes to demonstrate STDP weight updates.
* Port the subcircuit into ngspice or LTspice for mixed-signal designs.